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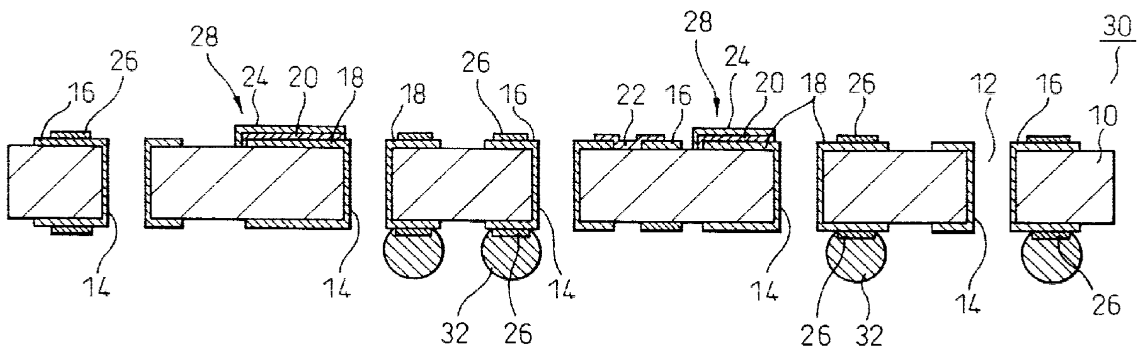
(54) **Interposer and semiconductor device using it**

(57) An interposer (30) is adapted to be used between a mounting board (36) and a semiconductor chip (50) which is to be mounted on the mounting board (36). The interposer (30) comprises: a heat-resistant insulator (10) having first and second surfaces, the insulator (10) being provided with a plurality of through-holes (12) opened at the first and second surfaces; wiring patterns (18) formed on the first and second surfaces of the insulator electrically connected to each other by means of a conductor (14) provided on an inner wall of at least one of the through-holes (12); and a capacitor (28). The capacitor (28) comprises first electrode (18) formed on the insulator (10) and having a connecting portion (14) formed on an inner wall of at least one of the other through-holes (12), a dielectric layer (20) formed on the first electrode (18) and a second electrode (24) formed on the dielectric layer (20).

Fig. 4



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Description

[0001] The present invention relates to an interposer for a semiconductor device, a method for producing the same and a semiconductor device including the same.

[0002] Capacitors are attached, for absorbing noise, to a multilayered circuit board carrying semiconductor chips. In the prior art, chip capacitors are attached to the exterior of the multilayered circuit board for this purpose.

[0003] However, the provision of the chip capacitors in the exterior of the multilayered circuit board is problematic in that the distance between the semiconductor chips and the chip capacitors is lengthened to deteriorate the noise absorbing capacity thereof, as decoupling capacitors, and the number of steps, for mounting a plurality of chip capacitors, is increased to increase the production cost. Also, there is a problem that the total size of a device which includes the chip capacitors is large.

[0004] The present invention has been made to solve the above problems in the prior art, and an object thereof is to provide an interposer for a semiconductor device excellent in noise absorbing capacity, small in size and low in production cost, a method for producing the same and a semiconductor device using the same.

[0005] According to the present invention, there is provided an interposer adapted to be used between a mounting board and a semiconductor chip which is to be mounted on the mounting board, the interposer comprising: a heat-resistant insulator having first and second surfaces, the insulator being provided with a plurality of through-holes opened at the first and second surfaces; wiring patterns formed on the first and second surfaces of the insulator electrically connected to each other by means of a conductor provided on an inner wall of at least one of the through-holes; and a capacitor comprising first electrode formed on the insulator and having a connecting portion formed on an inner wall of at least one of the other through-holes, a dielectric layer formed on the first electrode, and a second electrode formed on the dielectric layer.

[0006] Thus, the interposer of this invention incorporates a capacitor which can be located near to and directly below the semiconductor chip. Therefore, the capacitor can very effectively act as a decoupling capacitor.

[0007] Also, a plurality of capacitors can be made at the same time when the interposer is manufactured, so that the production cost can be reduced.

[0008] Also, a wiring pattern is patterned again on the interposer, so that a fine pattern can be formed. Therefore, due to such a rewiring pattern, it is possible to reduce one of the layers of the mounting board which constitutes a multi-layered board.

[0009] The capacitor is arranged on the insulator and in a vacant area between the wiring patterns. Thus, a plurality of capacitors can be formed utilizing vacant areas between the wiring patterns.

[0010] The interposer further comprises connecting bumps on the wiring patterns and on the second electrode, the connecting bumps being used for electrically connecting the interposer to the mounting board.

[0011] The insulator is made of silicon, glass, or a heat-resistant polyimide.

[0012] The capacitor comprises the first electrode formed on at least one of the first and second surfaces of the insulator, and the dielectric layer formed on the first electrode and the second electrode formed the dielectric layer. Thus, the opposing areas of the first and second electrodes can be enlarged, so that capacity of the capacitor can be increased.

[0013] According to another aspect of the present invention, there is provided a method of manufacturing an interposer adapted to be used between a mounting board and a semiconductor chip which is to be mounted on the mounting board, the method comprising: a step for forming a plurality of through-holes in a heat-resistant insulator having first and second surfaces, so that the through-holes are opened at the first and second surfaces; a step for forming a first conductor layer on the first and second surfaces and the inner walls of the through holes of the insulator; a step for patterning the first conductor layer to form wiring patterns on the first and second surfaces of the insulator and electrically connected to each other by means of the first conductor provided on the inner wall of at least one of the through-holes and to form a first electrode on the insulator so that the first electrode is electrically connected to the first conductor formed on the inner wall of at least one of the other through-holes; a step for forming a dielectric layer to cover the first electrode and the wiring pattern; a step for patterning the dielectric layer to form the dielectric layer on the first electrode; a step for forming a second conductor layer on the insulator to cover the dielectric layer; a step for patterning the second conductor layer to form a second electrode on the dielectric layer.

[0014] Thus, a plurality of capacitors can be made at the same time when the interposer is manufactured, so that the production cost can be reduced.

[0015] According to still further aspect of the present invention, there is provided a semiconductor device comprising: a mounting board; a semiconductor chip mounted on the mounting board by means of an interposer disposed therebetween, so that predetermined portions of the semiconductor chip are electrically connected to the mounting board through the interposer. The interposer has the construction mentioned above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016]

Figures 1 to 4 are cross-sectional views illustrating a process for manufacturing an interposer of this invention, wherein Fig. 1 illustrates a state of an insulator provided with through-holes, Fig. 2 illus-

trates a state that wiring patterns and first electrodes are formed, Fig. 3 illustrates a state that dielectric layers are formed, and Fig. 4 illustrates a state that second electrode layers are formed;

Figure 5 is schematic cross-sectional view of a semiconductor device;

Figure 6 illustrates another embodiment of an interposer of this invention;

Figure 7 illustrates still another embodiment of an interposer of this invention; and

Figure 8 illustrates a still further embodiment of an interposer of this invention.

[0017] The preferred embodiments of the present invention will be described in more detail below with reference to the attached drawings.

[0018] An interposer will be described together with a method for producing the same.

[0019] Fig. 1 illustrates a plate-like insulator 10.

[0020] A plurality of through-holes 12 having a diameter in a range from 30 to 300 μm are provided in the insulator 10 at a predetermined pattern by a YAG laser or an excimer laser.

[0021] Since a heat load is applied during the sputtering as described later, the insulator 10 must be heat-resistant. For example, a polished flat silicon substrate of 50 μm thick is preferably used as the insulator 10.

[0022] Alternatively, the insulator 10 may be glass or a heat-resistant polyimide resin. A glass substrate is preferable because of its surface smoothness. When a glass substrate is used as an insulator 10, it is preferable to polish the substrate to obtain a smooth and flat surface thereof and to make a thin substrate.

[0023] When glass is used as the insulator 10, the through-holes 12 may be provided by an etching method while using a mask, or by a sand blasting method while using a mask.

[0024] As the insulator 10, a silicon substrate or a glass substrate is more preferable than a resin substrate, such as made of polyimide, because the surface thereof can advantageously be made smooth and flat.

[0025] After that, sputtering and then electrolytic plating are carried out to form a first conductor layer (not shown) of copper, aluminum or others on front and back surfaces of the insulator 10, including inner walls of the through-holes 12.

[0026] A silicon substrate polished to have a mirror surface is favorably used when the first conductor layer is formed (particularly when a sputtering film is formed) because a first conductor layer of an extremely uniform thickness and free from irregularity can be formed.

[0027] Then, as shown in Fig. 2, the first conductor layer is patterned by a lithographic method to form wiring patterns 16 electrically connected to each other via conductor portions 14 formed in inner walls of some of the through-holes 12 and also to form first electrodes 18 electrically connected to each other via conductor portions 14 formed in inner walls of some of the through-holes 12.

[0028] Next, a dielectric layer 20 is formed on the surfaces of the insulator 10 and covering the wiring patterns 16 and the electrodes 18. Such a dielectric layer 2 can be formed by a sputtering process.

[0029] Thereafter, the dielectric layer 20 is patterned to leave predetermined patterns on the first electrodes 18.

[0030] The dielectric layer 20 is formed preferably of a ferroelectric substance, such as STO (strontium titanium oxide) or PZT (lead zirconium titanium) and therefore a capacitor having a high capacity is obtainable.

[0031] The thinner the dielectric layer 20, the larger the capacity of the capacitor. Since the underlayer, i.e., the first electrode 18 formed by patterning the first conductor layer, has a smooth surface having no irregularity as described above, it is possible to obtain a favorable dielectric layer 20 which is thin but free from defects such as pin holes or others.

[0032] As shown in Fig. 3, if the dielectric layer is left to connect adjacent wiring patterns 16 with each other, the dielectric layer can be used as a resistor 22.

[0033] Then, a second conductor layer (not shown) is formed on the surfaces of the insulator 10 while covering the dielectric layer 20 by sputtering or electrolytic plating.

[0034] Next, as shown in Fig. 4, the second conductor layer is patterned by a lithographic method so that second electrodes 24 are formed on the dielectric layer 20.

[0035] Thereafter, gold pads 26 are formed on the necessary portions of the wiring patterns 16, first electrodes 18 and second electrodes 24. The gold pads 26 can preferably be formed by plating or sputtering. Thus, an interposer 30 is completed. In this regard, the gold pads 26 are not indispensable.

[0036] The interposer 30 has a necessary number of capacitors 28 consisting of the first electrode 18, the dielectric layer 20 and the second electrode 24.

[0037] This interposer 30 may have solder bumps 32 on the gold pads 26 provided on a side to be mounted to a circuit board.

[0038] Fig. 5 schematically illustrates a semiconductor device 50 in which a semiconductor chip 34 is mounted to a circuit board 36 (including a package for the semiconductor device) via the interposer 30.

[0039] Reference numeral 38 denotes connecting bumps provided on the semiconductor chip 34; 40 denotes a power source line; and 42 denotes a ground line.

[0040] As described above, according to this embodiment, since the capacitors 28 incorporated in the interposer 30 are located directly beneath the semiconductor chip 34 and extremely close thereto, it functions well as a decoupling capacitor.

[0041] Also, since a plurality of capacitors 28 are incorporated into the interposer 30 together with the resistors 22 at the same time as the interposer 30 is manufactured, the production cost can be reduced.

[0042] If the capacitor 28 is unnecessary, the semi-

conductor chip 34 may be directly mounted onto the circuit board 36.

[0043] Since the wiring patterns 16 are laid out again on the interposer 30, fine patterns are obtainable. Also, due to this re-layout of the wiring pattern, it is substantially possible to reduce one of the layers of the mount board 36 which constitutes a multilayered substrate.

[0044] This embodiment has an advantage in that a number of capacitors 28 can be formed in a vacant space between the wiring patterns 16.

[0045] While the capacitors 28 are formed on a surface of the interposer 30 closer to the semiconductor chip 34 to be mounted in the embodiment described above, the capacitor 28 may be formed on a surface closer to the circuit board 36 as in another embodiment shown in Fig. 6 wherein the same reference numerals are used for denoting the same or corresponding parts.

[0046] This interposer may be manufactured in the same process as described above.

[0047] A further embodiment of the present invention is shown in Fig. 7 wherein the same reference numerals are used for denoting the same or corresponding parts.

[0048] According to this embodiment, dielectric layers 20, 20 are formed on first electrodes 18 provided on front and back surfaces of an insulator 10. On both the dielectric layers 20, 20 are formed second electrodes 24, 24 which are connected to each other via a conductor portion 14a formed in an inner wall of a through-hole 12a. The first electrodes 18 formed on the front and back surfaces of the insulator 10 are connected to each other via a conductor portion 14b formed in an inner wall of a through-hole 12b.

[0049] According to this embodiment, areas of both the electrodes 18, 24 of the capacitor 28 opposed to each other become larger to increase the capacity of the capacitor 28 to result in an interposer excellent in electric characteristics.

[0050] This interposer is also manufactured by the same process as described above because the dielectric layers 20 and the second conductor layers 24 are formed on the respective front and back surfaces of the insulator 10.

[0051] A further embodiment is shown in Fig. 8 wherein a dielectric layer 20 is provided also in the interior of a through-hole 12 to cover a conductor portion 14 connecting first electrodes 18 formed on front and back surfaces of the insulator 10 with each other, and second electrodes 24 are provided to cover all of the dielectric layer 20.

[0052] In this embodiment, areas of both the first and second electrodes 18, 24 opposed to each other become larger to increase the capacity of the capacitor 28. Since the capacitor is formed in the through-hole, it is unnecessary to provide a capacitor on the surface of the interposer. Thus, an increase in wiring density of the interposer as well as a reduction in the size of the interposer are achievable.

[0053] In Fig. 8, the same reference numerals are used for denoting the same or corresponding parts.

[0054] It should be understood by those skilled in the art that the foregoing description relates to only some of the preferred embodiments of the disclosed invention, and that various changes and modifications may be made to the invention. For example, a plurality of semiconductor chips 34 can be mounted on the interposer 30 to obtain a multi-tip module.

Claims

1. An interposer adapted to be used between a mounting board and a semiconductor chip which is to be mounted on the mounting board, the interposer comprising:

   a heat-resistant insulator having first and second surfaces, the insulator being provided with a plurality of through-holes opened at the first and second surfaces;
   wiring patterns formed on the first and second surfaces of the insulator electrically connected to each other by means of a conductor provided on an inner wall of at least one of the through-holes; and
   a capacitor comprising first electrode formed on the insulator and having a connecting portion formed on an inner wall of at least one of the other through-holes, a dielectric layer formed on the first electrode, and a second electrode formed on the dielectric layer.

2. An interposer according to claim 1, wherein the capacitor is arranged on the insulator and in a vacant area between the wiring patterns.

3. An interposer according to claim 1 or 2, further comprising connecting bumps on the wiring patterns and on the second electrode, the connecting bumps being used for electrically connecting the interposer to the mounting board.

4. An interposer according to any preceding claim, wherein the insulator is made of silicon, glass, or a heat-resistant polyamide.

5. An interposer according to any one of the preceding claims, wherein
   the capacitor comprises the first electrode formed on at least one of the first and second surfaces of the insulator, and the dielectric layer formed on the first electrode and the second electrode formed the dielectric layer.

6. An interposer according to any one of claims 1 to 4, wherein the capacitor comprises the first electrode, at least a part thereof being formed on the inner wall

of the through-hole, the dielectric layer formed on the first electrode and the second electrode formed the dielectric layer.

7. A method of manufacturing an interposer adapted to be used between a mounting board and a semiconductor chip which is to be mounted on the mounting board, the method comprising:

a step for forming a plurality of through-holes to a heat-resistant insulator having first and second surfaces, so that the through-holes are opened at the first and second surfaces;
a step for forming a first conductor layer on the first and second surfaces and inner walls of the through holes of the insulator;
a step for patterning the first conductor layer to form wiring patterns on the first and second surfaces of the insulator electrically connected to each other by means of the first conductor provided on the inner wall of at least one of the through-holes and to form a first electrode on the insulator so that the first electrode is electrically connected to the first conductor formed on the inner wall of at least one of the other through-holes;
a step for forming a dielectric layer to cover the first electrode and the wiring pattern;
a step for patterning the dielectric layer to form the dielectric layer on the first electrode;
a step for forming a second conductor layer on the insulator to cover the dielectric layer;
a step for patterning the second conductor layer to form a second electrode on the dielectric layer.

8. A method as set forth in claim 7, the method further comprising a step of forming connecting bumps on the wiring patterns and the second electrode.

9. A semiconductor device comprising:

a mounting board;
a semiconductor chip mounted on the mounting board by means of an interposer disposed therebetween, so that predetermined portions of the semiconductor chip are electrically connected to the mounting board through the interposer, the interposer comprising:

a heat-resistant insulator having first and second surfaces, the insulator being provided with a plurality of through-holes opened at the first and second surfaces;
wiring patterns formed on the first and second surfaces of the insulator electrically connected to each other by means of a conductor provided on an inner wall of at least one of the through-holes; and
a capacitor comprising a first electrode formed on the insulator and having a connecting portion formed on an inner wall of at least one of the other through-holes, a dielectric layer formed on the first electrode, and a second electrode formed on the dielectric layer.

Fig.1

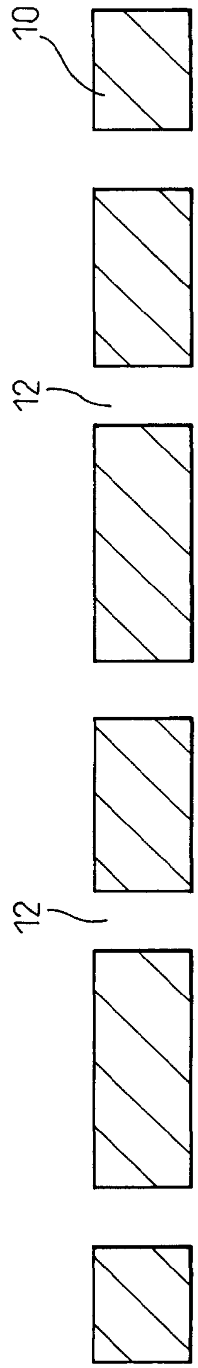
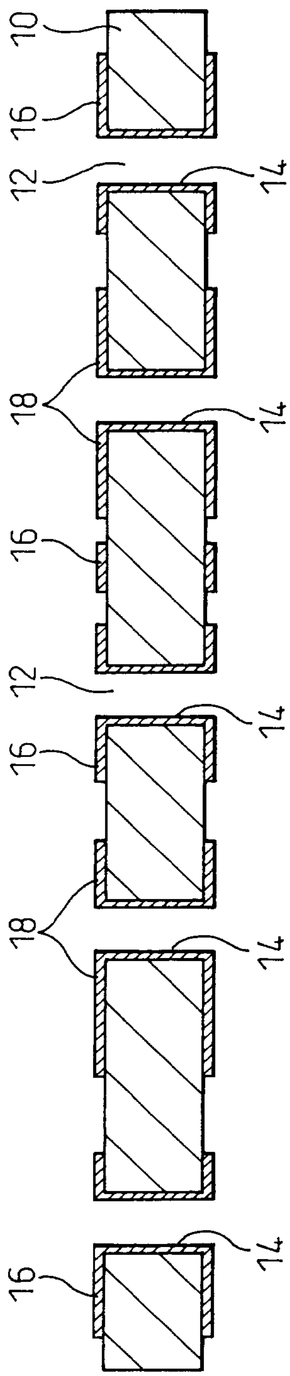


Fig.2



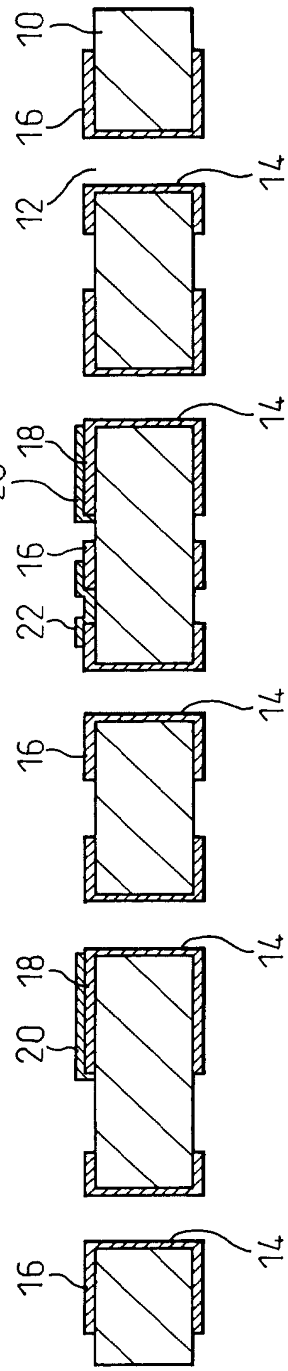


Fig.3

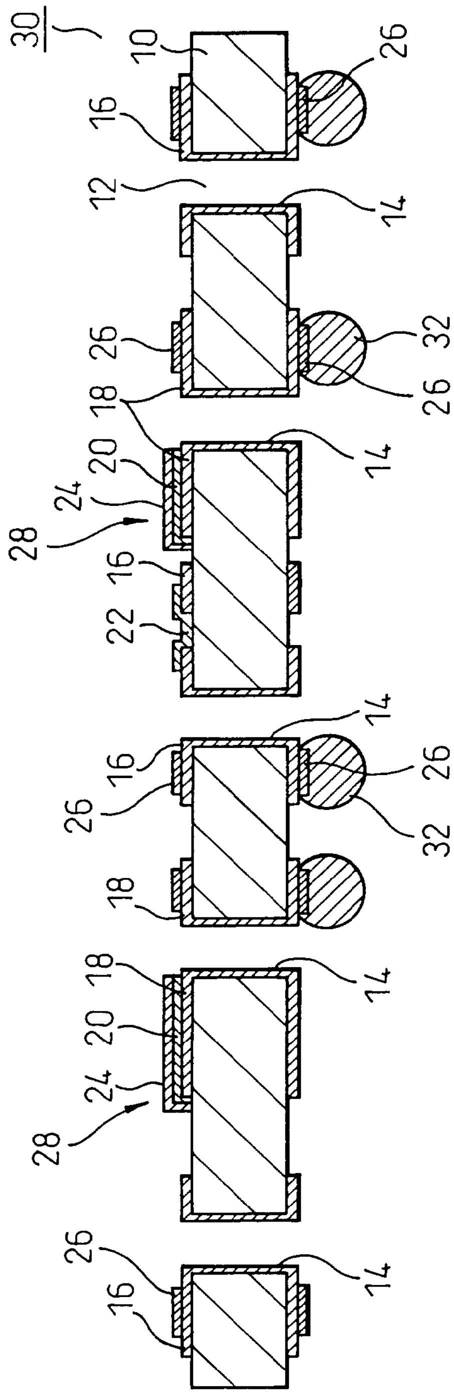


Fig. 4

Fig. 5

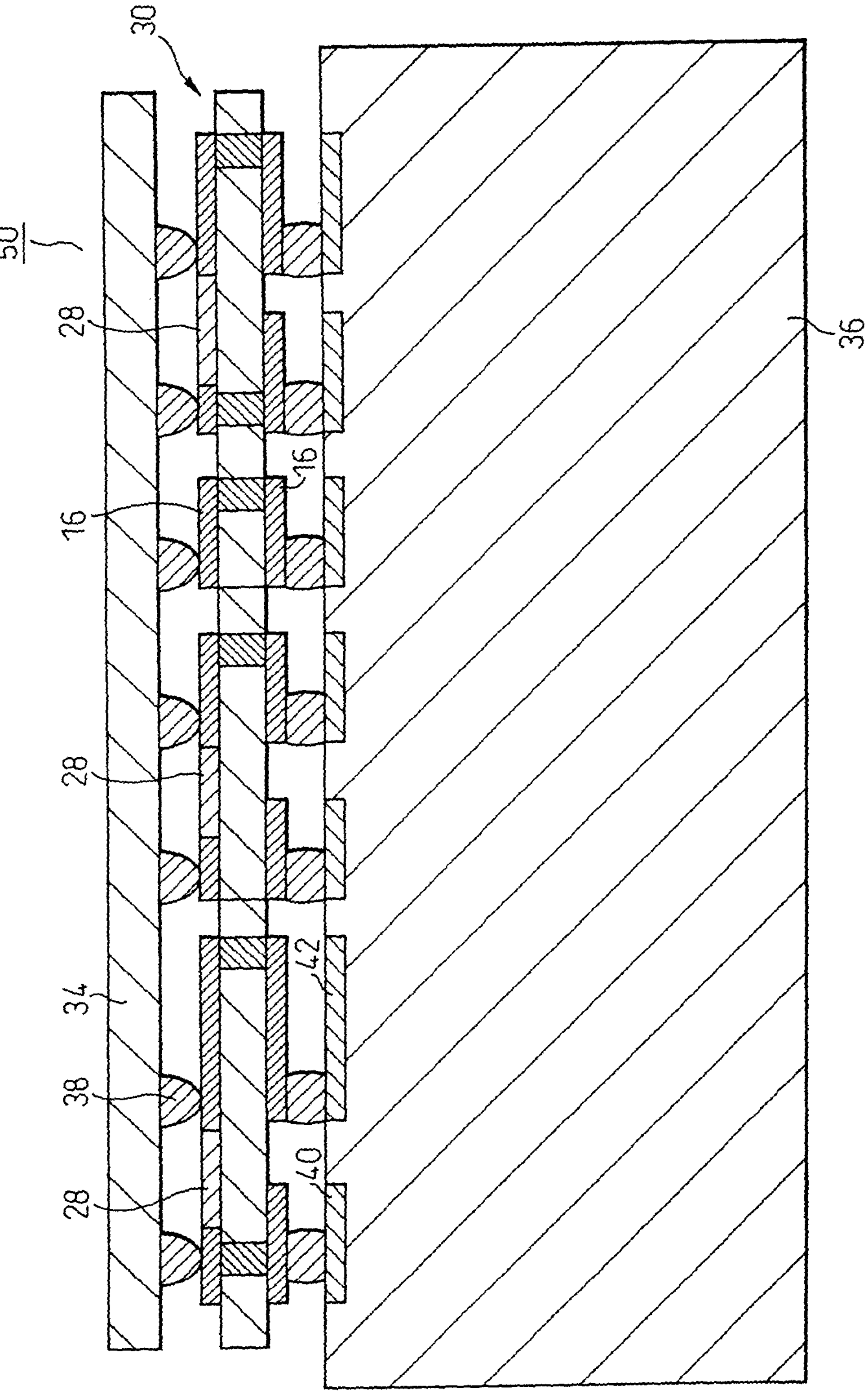


Fig.6

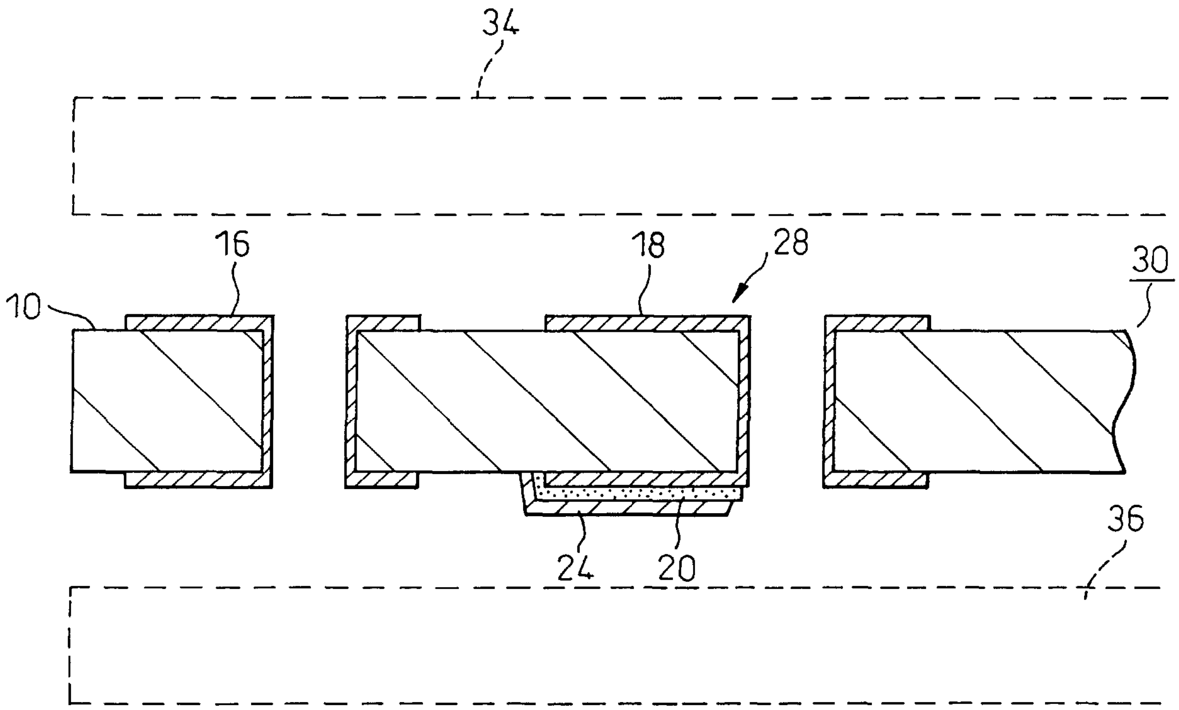


Fig.7

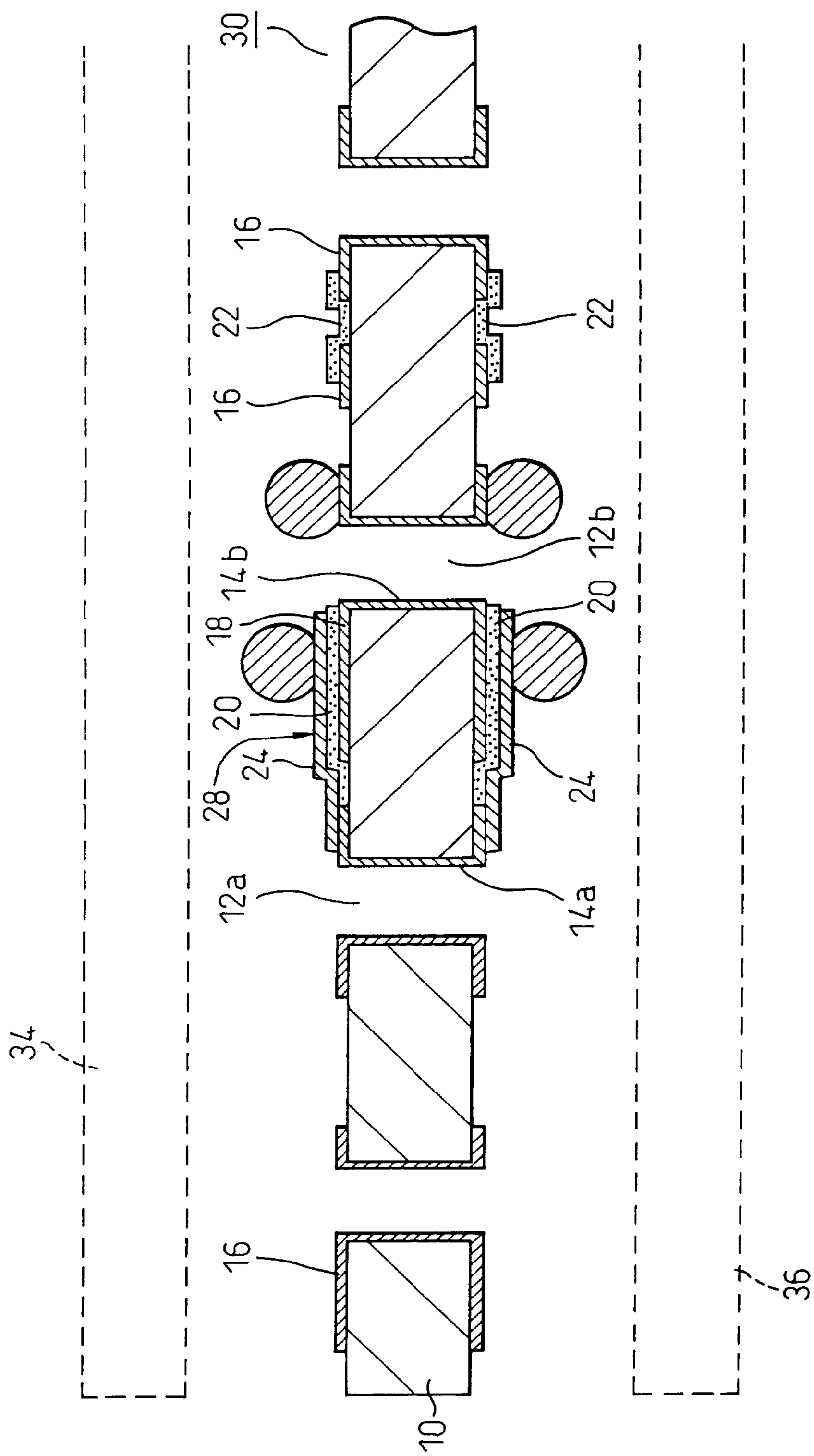


Fig.8